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# A 15 TO 45 GHZ DISTRIBUTED AMPLIFIER USING 3 FETS OF VARYING PERIPHERY

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## ABSTRACT

A 15 to 45 GHz GaAs MMIC distributed amplifier is described. The amplifier uses a unique configuration of three FETs of varying periphery. This configuration accommodates more FET periphery than a conventional distributed amplifier, resulting in higher gain and output power.

A high yield 0.25 μm gate technology has been developed. A 15-45 GHz amplifier using 0.25 μm gates has been demonstrated. The amplifier is fully monolithic - all bias circuitry and terminations are contained on a .035" x .069" (0.89 mm x 1.75 mm) chip. 5 dB gain has been demonstrated for a single amplifier stage.

Two extended bandwidth versions of the 3 FET amplifier of varying periphery were included in the same layout. 2 to 44 GHz and 15 to 50 GHz versions have both been demonstrated with 4 dB gain.

## INTRODUCTION

Since distributed amplifiers were first demonstrated successfully in MMICs [1], frequency ranges have been progressively extended to 40 GHz [2,3,4]. Unfortunately, as frequencies have been extended, gain has suffered. The present paper describes circuits with extended frequency bands (to 45 and 50 GHz). A unique distributed amplifier structure with only 3 FETs (each with a different periphery) has been developed. This structure allows for high frequency operation with improved gain and output power.

This distributed amplifier structure not only yields improved performance, but also allows for compact circuit layout - even when all bias circuitry is on the chip. As an example, the 2 to 44 GHz amplifier described below includes all bias circuitry on chip, yet is smaller than a 2 to 40 GHz amplifier described in the literature [4] that does not include bias circuitry.

Further size reductions are realized by increasing the low frequency cut-off of the amplifier. Distributed amplifiers are theoretically capable of operation down to dc, but in practice low frequency operation is limited by bias circuitry. By limiting low frequency operation to 15 GHz, bias circuitry can reduced in size dramatically, allowing chip size to be reduced. For example, the 15 to 45 GHz amplifier described below is about half the size of the 2 to 44 GHz version. Since most applications for these amplifiers only require operation above 18 GHz, limiting the amplifiers to operate above 15 GHz is justified.

## QUARTER MICRON GATE FETS

A high yield 0.25 μm gate micron gate process has been developed for a variety of mm-wave applications, including the amplifiers presented in this paper. The process development included a comprehensive study of developers and their interaction with exposed and unexposed electron beam resists. Gate lengths were measured on a field emission SEM which was concurrently checked with an NBS standard. The accuracy of the SEM was thus known to be within 5%.

Electrical performance and yield information from the processed wafers is very good. The yields of these wafers has been very good. The final front-side dc yield obtained on the circuits presented in this paper was 58%, indicating that gate yield is substantially higher. An SEM photo of a gate on of the 15 to 45 GHz amplifiers is shown in figure 1.

The FETs used in the amplifiers were made of VPE material with a doping of $3 \times 10^{17}$ $cm^{-3}$ and a contact layer of $2 \times 10^{18}$ $cm^{-3}$. The source-drain spacing is 2.5 μm. A $g_m$ of 180 ms/mm is typically achieved at $I_{dss}$. The pinch-off voltage for these devices is -2.5 volts. The I-V curve for a representative device with a 220 μm periphery is shown in Figure 2. The breakdown voltage is typically -16 volts.

## CIRCUIT STRUCTURE

The circuit diagram of the 15 to 45 GHz amplifier is shown in Figure 3. The FET nearest the input (FET1) is the smallest, the proceeding FETs increase in size. A total of 490 μm of periphery is accomodated by this circuit. The corresponding conventional 4 FET

distributed amplifier can only accomodate 330 μm of periphery.

Increased periphery ideally increases gain, but in practice there a limit to the amount of periphery that a distributed amplifier can accommodate, regardless of the number of FETs [5]. As periphery increases, not only does gain increase, but gate line losses also increase. As the gate line losses increase, the input drive to the FETs decreases, with the lowest drive level to the FET farthest from the input. As periphery increases, eventually the input drive to the last FET becomes so small that the FET attenuates the output signal. Thus there is a limit to amount of FET periphery a distributed amplifier can accommodate.

The same periphery limiting mechanism occurs in the circuit in Figure 4. The signal drive level for FET3 is reduced by gate line losses related to the total periphery. Since the periphery of FET3 is the largest, it can make up for lower input levels with its higher gain. Thus the 3 FET amplifier with varying periphery can accommodate more periphery.

Increasing the FET periphery of a distributed amplifier can also increase the maximum output power level. One of the power limiting mechanisms in a distributed amplifier is drain current limiting. For a given FET type, there is a maximum rf output current available per unit periphery. To increase output current in an amplifier, periphery must be increased. In a conventional distributed amplifier current typically limits first in the FET nearest the output. In Figure 3, the FET nearest the output has the largest periphery. Thus current limiting in the last FET is forestalled. In the 3 FET amplifier with varying periphery current limiting occurs at higher power levels because total periphery is larger and because periphery is added where it is needed the most, at the FET nearest the output.

## FABRICATION

The circuits described above were fabricated on 3" GaAs wafers. The details of the FETs used are described above. Polyimide passivation is used. MIM capacitors with 3000 Å of $Si_3N_4$ are used. Two types of resistors are used. For low value resistors (such as gate and drain terminations) TiPt is used. For large value resistors (2 kΩ gate bias resistors) open gate FET resistors are used. Inductances are realized with transmission lines 10 μm wide and 3 μm thick. Plasma etched via holes are 50 μm by 50 μm, and are under 150 μm by 150 μm via pads. The wafer is thinned to 100 μm.

The 15 to 45 GHz amplifier chip is shown in figure 4a. The complete chip measures .035" by .069" (.89 mm by 1.75 mm).

## RESULTS

The measured gain of the 15 to 45 GHz amplifier is shown in figure 4b. A gain of 5 dB was achieved from 15 to 45 GHz at $I_{dss}$. The input and output return losses are better than 10 dB over most of the band, although they are as poor as 6 dB at some points. There is a measurement discontinuity at 40 GHz, where measurement apparatus were changed. Below 40 GHz measurements were made with a coax based scalar analyzer, above 40 GHz measurements were made with waveguide based vector analyzer.

No additional matching external to the chips was done. All bias circuitry, gate and drain terminations, and blocking capacitors are included on chip.

The output power for the 15 to 45 GHz amplifier was also measured, and is shown in figure 4c. At 1 dB compression, there is 14 dBm of output from 15 GHz to 38 GHz, with peaks of 15 dBm at several points. Above 38 GHz output power rolls off, reaching a low of 7 dBm at 45 GHz

To demonstrated broader bandwidths of operation, two other amplifiers were included in the layout, a 2 to 45 GHz amplifier and 15 to 50 GHz amplifier. Chip photos and performance curves for these amplifiers are shown in figures 5 and 6 respectively. Better than 4 dB gain was achieved from both of these amplifiers over their respective bands. The 1 dB compressed power output is better than 12 dBm for the 2 to 44 GHz amplifier up to 39 GHz. The 1 dB compressed output power for the 15 to 50 GHz version is better than 11 dBm from 14 to 45 GHz, with a peak of 16 dBm at 27 GHz.

## CONCLUSION

A 15 to 45 GHz distributed amplifier with 3 FETs of varying periphery has been demonstrated. 5 dB gain was achieved from 15 to 45 GHz from a single amplifier stage. The 1 dB compressed output power was 14 dBm over a 15 to 38 GHz band.

In order to demonstrate the performance of the circuit structure over broader bandwidths, two other amplifier versions were included in the layout. One showed 4 dB gain from 2 to 44 GHz, and the other had 4 dB gain from 15 to 50 GHz.

## ACKNOWLEDGEMENTS

The authors would like to thank P. Katzin, D. Janes, and M. Weiler for assistance in FET modelling, A. Scorza and P. Hatch for layout, M. Miller for processing, N-L. Wang, S. Sengupta, and G. Chu for test fixtures, D. Kelly, S. Nash, and D. Satterthwaite for measurements, and L. Reynolds for numerous useful discussions.

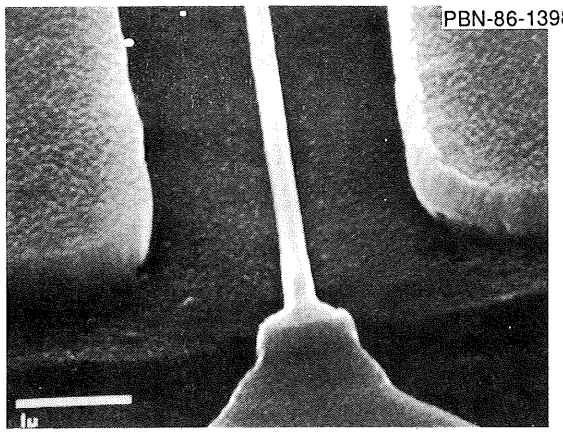


Figure 1. Quarter Micron Gate FET

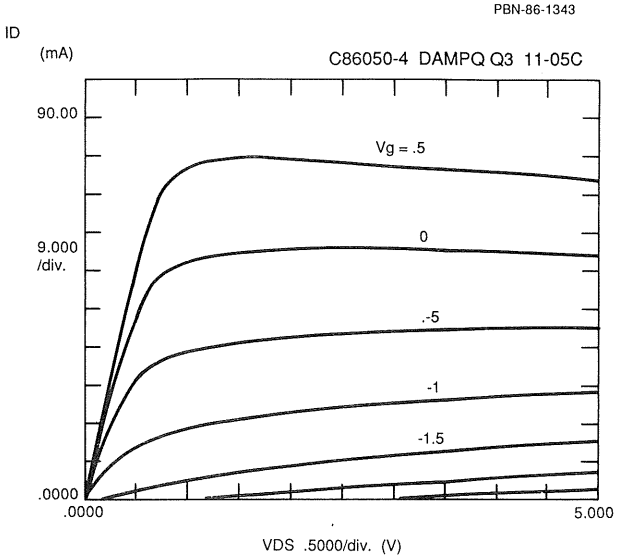


Figure 2. I-V Curve for a 0.25 μm x 220 μm Gate FET

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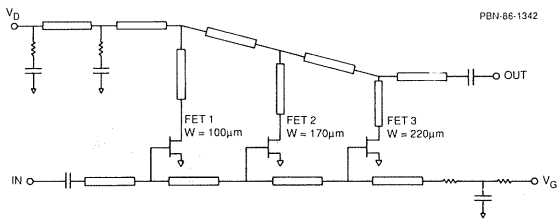
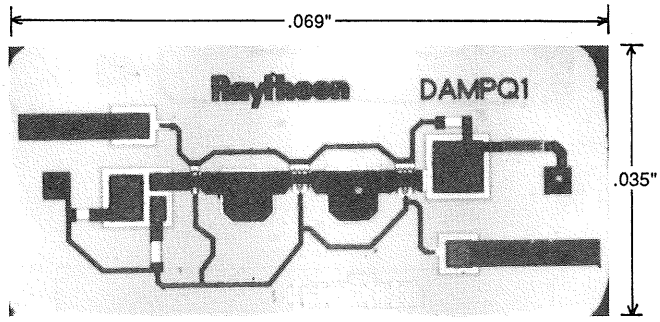
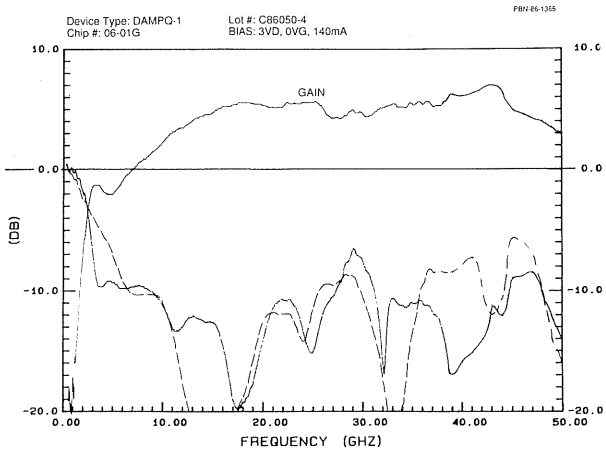



Figure 3. Schematic for the 15-45 GHz 3 FET Distributed Amplifier




(a)

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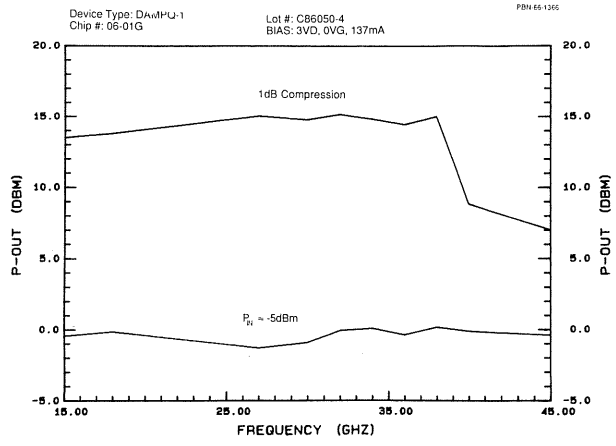
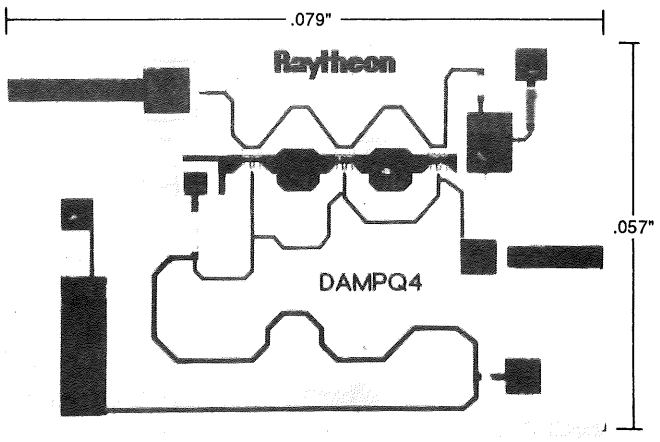



(c)

Figure 4. 15-45 GHz 3 FET Amplifier (a) chip photo (b) small signal performance (c) 1 dB Compressed Output Power

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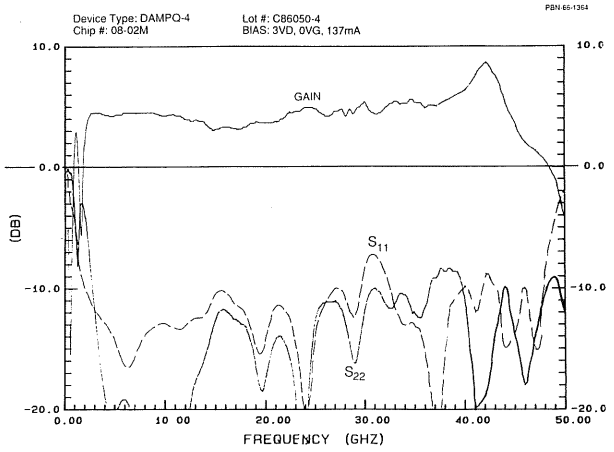


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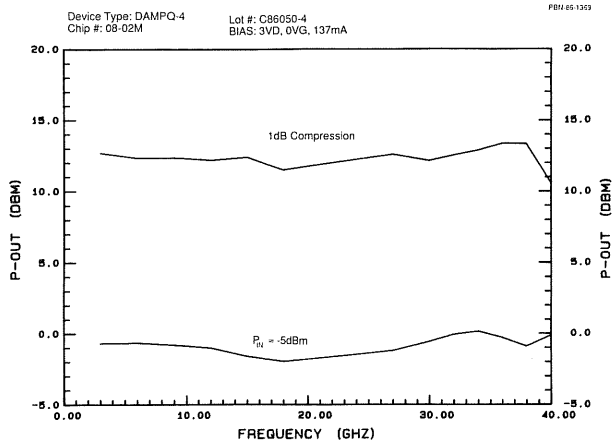
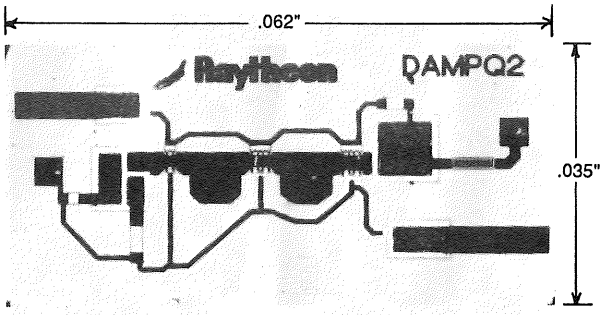
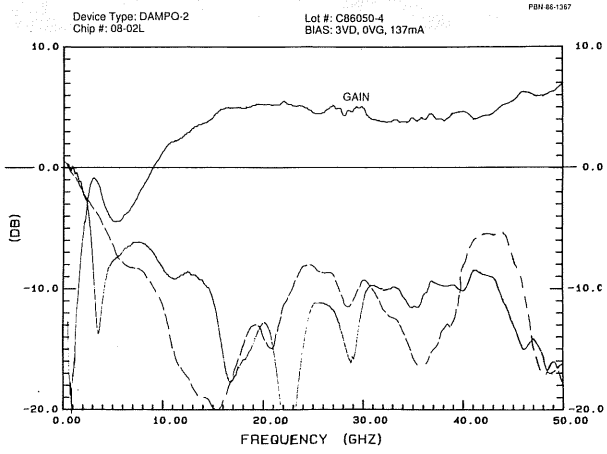



(c)

Figure 5. 2-44 GHz 3 FET Amplifier
(a) chip photo (b) small signal performance (c) 1 dB Compressed Output Power




(a)

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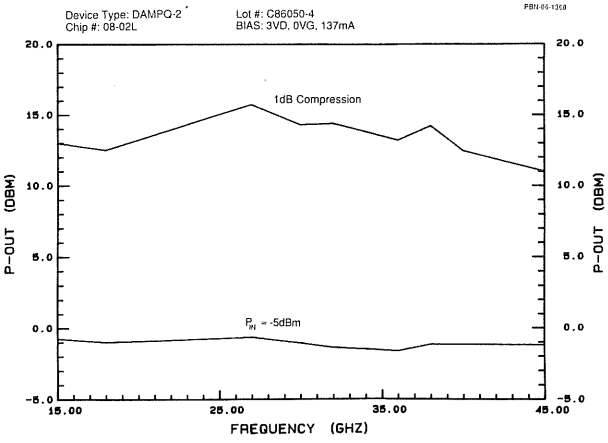


(c)

Figure 6. 15-50 GHz 3 FET Amplifier
(a) chip photo (b) small signal performance (c) 1 dB Compressed Output Power

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